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322356(28)

B. E. (Third Semester) Examination, Nov.-Dec. 2021

(New Scheme)

(CSE Branch)

DIGITAL ELECTRONICS & LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Attempt all units. Part (a) of each unit is compulsory carrying 2 marks. Attempt any two parts from parts (b), (c) and (d) carrying 7 marks each.*

Unit-I

1. (a) State De Morgan's theorem. 2

   (b) Minimize the following using K-map 7

$$f(A, B, C) = \sum m(1, 2, 3, 5, 7)$$

(c) Simplify the expression

$$Y = \Pi(0, 1, 4, 5, 6, 8, 9, 12, 13, 14)$$ 7

(d) Simplify Boolean function : 7

$$F(A, B, C, D) = \sum m(1, 3, 7, 11, 15) + \sum d(0, 2, 5)$$

Unit-II

2. (a) Define "fan in" and "fan out". 2

(b) Describe Resistor Transistor Logic (RTL) with it's logic operation with relevant diagram. 7

(c) Explain ECL with circuit diagram. 7

(d) Draw and explain TTL NAND gate. 7

Unit-III

3. (a) Define combinational circuit. 2

(b) Describe full adder circuit. Design full adder with two half adder. 7

(c) Design a 4 bit binary to gray code converter. 7

(d) Describe multiplexer and demultiplexer circuit with diagram. 7

Unit-IV

4. (a) Define Asynchronous and synchronous counter. 2

(b) Describe Master slave JK flip-flop in detail. 7

(c) Describe D flip-flop and T flip-flop with truth table and block diagram. 7

(d) Describe serial input parallel output and serial input serial output. 7

Unit-V

5. (a) Define state diagram. 2

(b) Describe mealy state and moore state machine in detail. 7

(c) Draw and explain PLA. 7

(d) Short notes on static RAM and Dynamic RAM. 7